CLAIMS

What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. A memory device comprising,

an apparatus for reading data from a programmable conductor random access memory cell, said apparatus comprising:

an access circuit for coupling said memory cell between an addressed and activated word line and an addressed and activated bit line during a read operation;

a sense amplifier coupled to said addressed and activated bit line for sensing a logical state of said memory cell; and

preventing circuitry for preventing said memory cell from being refreshed in response to said read operation.

2. The memory device of claim 1, wherein said access circuit is a transistor circuit and said preventing circuitry causes said activated word line to be deactivated after a logical state of said memory cell is transferred to said activated bit line and before said sense amplifier senses a logical state of said memory cell.

3. The memory device of claim 2, wherein said preventing circuitry comprises a transistor which causes said activated word line to be deactivated.

4. The memory device of claim 3, wherein said transistor is serially connected between said word line and a driver for said word line and is turned on during said read operation and turned off to deactivate said row line.

5. The memory device of claim 3, wherein said transistor is connected between said word line and ground and is turned off during said read operation and is turned on to deactivate said word line.

6. The memory device of claim 1, wherein said preventing circuitry comprises a transistor serially connected between an activated bit line and a sense amplifier associated with the activate bit line, said serially connected transistor being turned on during a read operation and turned off before said memory cell can be refreshed.

7. The memory device of claim 1, wherein said preventing circuitry causes said activated word line to be deactivated a predetermined amount of time after said memory cell begins to transfer a logical state to said activated bit line.

8. The memory device of claim 7, wherein said sense amplifier further comprises a first sense amplifier portion and a second sense amplifier portion.

9. The memory device of claim 8, wherein said predetermined amount of time is after said first sense amplifier portion is activated and before said second sense amplifier portion is activated.

10. The memory device of claim 8, wherein said first sense amplifier portion is a N-sense amplifier, and said second sense amplifier portion is a P-sense amplifier.

11. The memory device of claim 1 further comprising:

a pre-charge circuit for pre-charging the addressed and activated bit line and an another bit line, wherein said addressed and accessed bit line and said other bit line are coupled to the sense amplifier.

12. The memory device of claim 11, wherein said pre-charge circuit pre-charges the addressed and activated bit line and the another bit line prior to the sense amplifier sensing said addressed and activated bit line.

13. An system comprising,

a processor; and

a memory, said memory further comprising,

an apparatus for reading data from a programmable conductor random access memory cell, said apparatus comprising:

an access circuit for coupling said memory cell between an addressed and activated word line and an addressed and activated bit line during a read operation;

a sense amplifier coupled to said addressed and activated bit line for sensing a logical state of said memory cell; and

preventing circuitry for preventing said memory cell from being refreshed in response to said read operation.

14. The system of claim 13, wherein said access circuit is a transistor circuit and said preventing circuitry causes said activated word line to be deactivated after a logical state of said memory cell is transferred to said activated bit line and before said sense amplifier senses a logical state of said memory cell.

15. The system of claim 14, wherein said preventing circuitry comprises a transistor which causes said activated word line to be deactivated.

16. The system of claim 15, wherein said transistor is serially connected between said word line and a driver for said word line and is turned on during said read operation and turned off to deactivate said row line.

17. The system of claim 15, wherein said transistor is connected between said word line and ground and is turned off during said read operation and is turned on to deactivate said word line.

18. The system of claim 13, wherein said preventing circuitry comprises a transistor serially connected between an activated bit line and a sense amplifier associated

with the activate bit line, said serially connected transistor being turned on during a read operation and turned off before said memory cell can be refreshed.

19. The system of claim 13, wherein said preventing circuitry causes said activated word line to be deactivated a predetermined amount of time after said memory cell begins to transfer a logical state to said activated bit line.

20. The system of claim 19, wherein said sense amplifier further comprises a first sense amplifier portion and a second sense amplifier portion.

21. The system of claim 20, wherein said predetermined amount of time is after said first sense amplifier portion is activated and before said second sense amplifier portion is activated.

22. The system of claim 20, wherein said first sense amplifier portion is a N-sense amplifier and said second sense amplifier portion is a P-sense amplifier.

23. The system of claim 13 further comprising:

a pre-charge circuit for pre-charging the addressed and activated bit line and an another bit line, wherein said addressed and accessed bit line and said other bit line are coupled to the sense amplifier.

24. The system of claim 23, wherein said pre-charge circuit pre-charges the addressed and activated bit line and the another bit line prior to the sense amplifier sensing said addressed and activated bit line.

25. A method for reading data from a programmable conductor random access memory cell, said method comprising:

activating an addressed word line containing said programmable conductor random access memory cell and transferring a logical value in said cell to an associated addressed bit line;

deactivating said addressed word line; and

sensing a logical value transferred to said bit line after said word line is deactivated.

26. The method of claim 25, wherein said deactivating takes place a predetermined amount of time after said activating.

27. The method of claim 25, wherein said sensing further comprises,

activating a first sense amplifier unit; and

activating a second sense amplifier unit a second predetermined time after said activating of said first sense amplifier unit.

28. The method of claim 25, wherein said deactivating takes place a first predetermined amount of time after said activating of an addressed word line.

29. The method of claim 28, wherein said first predetermined amount of time is after said activating of said first sense amplifier unit and before said activating of said second sense amplifier unit.

30. The method of claim 28, wherein said first predetermined amount of time is before said activating of said first sense amplifier unit and before said activating of said second sense amplifier unit.

31. A method for reading data from a programmable conductor random access memory cell, said method comprising:

activating an addressed word line containing said programmable conductor random access memory cell and transferring a logical value in said cell to an associated addressed bit line;

switching off an isolation transistor located on the associated addressed bit line and serially connecting a sense amplifier and said cell;

sensing a logical value transferred to said bit line after said word line is deactivated.

32. The method of claim 31, wherein said switching off takes place a predetermined amount of time after said activating.

33. The method of claim 31, wherein said sensing further comprises,

activating a first sense amplifier unit; and

activating a second sense amplifier unit a second predetermined time after said activating of said first sense amplifier unit.

34. The method of claim 32, wherein said switching off takes place a first predetermined amount of time after said activating of an addressed word line.

35. The method of claim 34, wherein said first predetermined amount of time is after said activating of said first sense amplifier unit and before said activating of said second sense amplifier unit.

36. The method of claim 34, wherein said first predetermined amount of time is before said activating of said first sense amplifier unit and before said activating of said second sense amplifier unit.

37. A method for reading data from a programmable conductor random access memory cell, said method comprising:

pre-charging a first bit line coupled to the programmable conductor random access memory cell, said memory cell including a programmable conductor memory element;

pre-charging a second bit line;

increasing voltage on said first bit line;

switching on an access transistor of said cell to couple the programmable conductor memory element to said first bit line;

switching off the access transistor of said cell to decoupling the programmable conductor memory element from said first bit line;

sensing voltage on said first bit line and said second bit line to determine a logical state of said programmable conductor memory element;

wherein said switching off is performed before said sensing.

38. A method for reading data from a programmable conductor random access memory cell, said method comprising:

switching on an isolation transistor to couple a first bit line to a sense amplifier, said first bit line also coupled to a programmable conductor memory element of the programmable conductor random access memory cell;

pre-charging said first bit line;

pre-charging a second bit line;

increasing voltage on said first bit line;

switching off said isolation transistor to decouple said programmable conductor memory element from said sense amplifier;

sensing voltage on said first bit line and said second bit line to determine a logical state of said programmable conductor memory element;

wherein said switching off is performed before said sensing.